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2818

Docket No.: INF 10391

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By: _____ Date: July 1, 2002

#13 I.D.S.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Peter Pöchmüller
Applic. No.	:	09/718,937
Filed	:	November 22, 2000
Title	:	Integrated Memory Having Memory Cells and Reference Cells
Examiner	:	Thong Q Le - Art Unit: 2818

Date of Notive of Allowance: March 29, 2002

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,844,832 (Kim), dated December 1, 1998;

German Published, Non-Prosecuted Patent Application DE 42 26 070 A1 (Nakayama et al.), dated June 9, 1993, semiconductor memory device having a redundancy circuit and testing method for checking whether or not the redundancy circuit is used.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

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It is believed that the enclosed prior art is less pertinent than the prior art previously submitted and cited by the Examiner. Kindly place the references in the Patent Office file wrapper.

Respectfully submitted,

For Applicant

Date: July 1, 2002

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